The Optimizing Tensor Contraction Engine

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Memory-Minimal Forms (Loop Fusion)



Effect of Different Optimizations

<u>AO-to-MO Transform:</u> N=150, V=140, Memory = 2GB

 $B(a,b,c,d) = \sum_{p,q,r,s} C1(s,d) \times C2(r,c) \times C3(q,b) \times C4(p,a) \times A(p,q,r,s)$

Optimizations included & omitted	Total Disk I/O time (secs)	Total Execution Time (secs)
Fusion + Optimizing Tiling	248.43	954.87
No Fusion, Optimizing Tiling	747.83	1261.95
No Fusion, Tile size = 4 th root of memorySize/3	1240.85	1957.18

Measurements were taken on an Itanium 2 System

Pseudo Codes for AO-to-MO Transform

Read C4, C3, C2, C1 FOR s_{T} FOR r_{T} FOR q_T FOR p_T Read A FOR a, s_I , r_I , q_I , p_I $T1[a,s_{I},r_{I},q_{I}] += C4[p,a] *$ $A[p_I,q_I,r_I,s_I]$ FOR a, s_I , r_I , q_I , b $T2[a,b,s_{I},r_{I}] += T1[a,s_{I},r_{I},q_{I}] *$ C3[q,b]FOR a, s_{I} , r_{I} , b, c $T3[a,b,c, s_{I}] += T2[a,b,s_{I},r_{I}] *$ C2[r,c]Write T3 FOR a_T FOR S_T Read T3 FOR a_{I} , b, c, s_{I} , d $B[a_{I},b,c,d] += T3[a_{I},b,c,sI] *$ C1[s,d]Write B

FOR aT Read C4 FOR rT, sT Read A FOR al, p, q, rl, sl T1[aI,q,rI,sI] += C4[p,aI] *A[p,q,rI,sI] Write T1 FOR aT, bT Read C3 FOR rT Read T1 FOR s, al, bl, q, rl T2[aI,rI,s,bI] += T1[aI,q,rI,s] *C3[q,bI]Write T2 Read C2, C1 FOR aT, bT Read T2 FOR c, r, s, aI, bI T3[aI,s,bI,c] += T2[aI,r,s,bI] *C2[r,c]Write T3 FOR aT. bT Read T3 FOR c, d, s, aI, bI B[aI,bI,c,d] += T3[aI,s,bI,c] *C1[s,d]Write B

Loop Fusion + Optimizing Tiling No Fusion, Optimizing Tiling

FOR aT, pT Read C4 FOR qT, rT, sT Read T1 Read A FOR al, pl, ql, rl, sl T1[aI,qI,rI,sI] += C4[pI,aI] *A[pI,qI,rI,sI] Write T1 FOR aT, bT, qT Read C3 FOR rT Read T2 Read T1 FOR s. al. bl. al. rl T2[aI,rI,s,bI] += T1[aI,qI,rI,s] *C3[qI,bI] Write T2 Read C2, C1 FOR aT, bT Read T2 FOR c, r, s, aI, bI T3[aI,s,bI,c] += T2[aI,r,s,bI] *C2[r,c]Write T3 FOR aT, bT Read T3 FOR c, d, s, aI, bI B[aI,bI,c,d] += T3[aI,s,bI,c] *C1[s,d]Write B No Fusion, Standard Tiling

CCSD Performance Itanium 2 Cluster

900 Megahertz Intel Itanium 2 processors, 4GB RAM		Sequential		4 Processors		16 Processors	
		CPU	Wall	CPU	Wall	CPU	Wall
	Native NWChem	1440	1440	389	389	102	102
	Scale			3.7		14.12	
Benzene	Prototype TCE	97.6	97.6	49.5	49.5	46	46
(Medium)	Scale			1.97		2.12	
	Optimizing TCE	48.5	48.5	15.6	15.6	13.3	13.3
	Scale			3.12		3.65	
	Native NWChem	2865	2865	806	806	212	212
	Scale			3.55		13.5	
Benzene	Prototype TCE	611	665	293	297	282	282
(Large)	Scale			2.24		2.36	
	Optimizing TCE	300	300	120	120	60.1	60.1
	Scale			2.5		4.99	

All times are in seconds

On the Drawing Board...

- More flexibility in sequencing and controlling optimizations
- Global factorization (across equations)
 - Complex problem
- Improving parallel code generation
 - Overlap of Communication and Computation
 - Multi-level parallelism
 - Threads
 - Multiple loosely coupled tasks
- More sophisticated performance models
- Develop approximate algorithms for opt.
 - Address situations where exhaustive search too expensive
 - i.e. Deliver best result spending at most 3 min on code gen.
 - ... or 60 min ... or 3 days ...
- Generalizations beyond electronic structure